ABSTRACT OF THE DISCLOSURE

P wells (11, 12) having different impurity profiles are adjacently formed in a surface (50S) of a semiconductor substrate (50). A P-type layer (20) having lower resistivity than the P wells (11, 12) is formed in the surface (50S) across the P wells (11, 12), so that the P wells (11, 12) are electrically connected with each other through the P-type layer (20). Contacts (31, 32) fill in contact holes (70H1, 70H2) formed in an interlayer isolation film (70) respectively in contact with the P-type layer (20). The contacts (31, 32) are connected to a wire (40). The wire (70) is connected to a prescribed potential, thereby fixing the P wells (11, 12) to prescribed potentials through the contacts (31, 32) and the P-type layer (20). Thus, the potentials of the wells can be stably fixed and the layout area of elements for fixing the aforementioned potentials can be reduced.